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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,410	01/28/2004	Cheon-Su Lee	8021-198 (SS-19354-US)	4171

22150 7590 10/21/2005

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EXAMINER	
DALEY, CHRISTOPHER ANTHONY	
ART UNIT	**PAPER NUMBER**
2111	

DATE MAILED: 10/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/766,410	LEE, CHEON-SU	
	Examiner	Art Unit	
	Christopher A. Daley	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6,8,11 and 14-17* is/are rejected.

7)☒ Claim(s) *5,7,9,10,12, 1nd 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 17 are pending.

Specification

2. The disclosure is objected to under 37 CFR 1.71, as being so incomprehensible as to preclude a reasonable search of the prior art by the examiner. For example, the following items are not understood: For example, the applicant describes one embodiment of the invention as follow:

> According to an embodiment of the present invention, a method arbitrates a system bus that is shared by a CPU, which is a first master device, and second and third master devices. A first bus occupancy rate for each of the CPU and the second and third master devices and a variable bus occupancy rate are stored. A second bus occupancy rate for the CPU, which is a sum of the first bus occupancy rate for the CPU and the variable bus occupancy rate, and the first bus occupancy rates for the second and third master devices are applied to a bus arbiter in response to the activation of an interrupt signal provided to the CPU. In response to the inactivation of the interrupt signal, a third bus occupancy rate for the CPU, which is obtained by subtracting the variable bus occupancy rate from the first bus occupancy rate for the CPU, and the first bus occupancy rates for the second and third master devices are applied to the bus arbiter.

A suggested correction is to point the illustration in figure 3 in a table to clearly communicate what constitutes the occupancy rate value for all the masters involved.

Since a similar format is used to describe all the embodiments, similar correction is requested on all presented embodiments.

Applicant is required to submit an amendment, which clarifies the disclosure so that the examiner may make a proper comparison of the invention with the prior art.

Applicant should be careful not to introduce any new matter into the disclosure (i.e., matter which is not supported by the disclosure as originally filed).

A shortened statutory period for reply to this action is set to expire ONE MONTH or THIRTY DAYS, whichever is longer, from the mailing date of this letter.

Claim Rejections - 35 USC § 112

3. Claims 1,2,3,4,6,8,11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the following limitations

applying a second bus occupancy rate for the CPU, which is a sum of the first bus occupancy rate for the CPU and the variable bus occupancy rate, and the first bus occupancy rates for the second and third master devices to a bus arbiter, in response to an activation of an interrupt signal provided to the CPU;

There is confusion as to the value of the CPU occupancy rate. For the purposes of applying prior art, the value of the CPU occupancy rate is the first bus occupancy rate for the CPU and the variable bus occupancy rate.

Claim 1 also recites applying a third bus occupancy rate for the CPU, which is obtained by subtracting the variable bus occupancy rate from the first bus occupancy rate for the CPU, and the first bus occupancy rates for the second and third master devices to the bus arbiter, in response to an inactivation of the interrupt signal;

There is confusion as to the value of the CPU occupancy rate. For the purposes of applying prior art, the value of the CPU occupancy rate is subtracting the variable bus occupancy rate from the first bus occupancy rate for the CPU.

Claims 2 – 3 contain said limitations and similar correction is required.

Claim 4 recites the following limitation:

a bus arbiter receiving either a second bus occupancy rate for the CPU, which is a sum of the first bus occupancy rate for the CPU and the variable bus occupancy rate, or a third bus occupancy rate for the CPU, which is obtained by subtracting the variable bus occupancy rate from the first bus occupancy rate for the CPU, in response to a privilege mode signal generated by the CPU, receiving the first bus occupancy rates for the second and third master devices, and controlling a priority for use of the system bus in accordance with received bus occupancy rates for the CPU and the second and third master devices.

There is confusion as to the value of the CPU occupancy rate. For the purposes of applying prior art, the value of the CPU occupancy rate is subtracting the variable bus occupancy rate from the first bus occupancy rate for the CPU.

Claims 6,8 and 11 also comprises said limitation and similar correction is required.

4. Claims 5,7,9,10,12,and 13 are objected to, as they are dependent on an independent claim that has been rejected.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 14 – 17 are rejected under 35 U.S.C. 102(b) as being anticipated by LaBerge (US6654833).

7. As to claim 14, LaBerge discloses A PCI bus system comprising: a PCI bus coupled to a plurality of slots; (figure 2)

a host device coupled to the PCI bus, the host device controlling the PCI bus system;

(LaBerge teaches that host device 34 of figure 2 is a bus controller that is coupled to PCI bus 38 of figure 2)

a device storing bus occupancy rates for a plurality of cards inserted into respective slots and a variable bus occupancy rate for increasing or decreasing the bus occupancy rates;

(LaBerge teaches that register 63 of figure 5 comprises said rates, COL. 4, lines 36 – 59).

and a bus arbiter controlling a priority for use of the PCI bus in accordance with the bus occupancy rates for the cards in response to interrupt signals generated by the cards.

(LaBerge teaches of bus arbiter 42 of figure 2 that comprises the elements illustrated in figure 5 that would respond to the interrupts from processor 32, COL. 2, lines 32 – 45).

8. As to claim 15, LaBerge discloses The PCI bus system of claim 14, wherein the host device is a PCI bridge circuit.

(LaBerge teaches that host device 34 of figure 2 is a PCI bridge, COL. 2, lines 35 – 41).

9. As to claim 16, LaBerge discloses The PCI bus system of claim 14, wherein each card is one of a graphic card, a network card, and a sound card.

(LaBerge teaches in figure 2 a display controller 43, which comprises a graphics card, a modem 46 , that comprises a network card, and an I/O expansion bus 40 that may drive a sound card).

10. As to claim 17, LaBerge discloses a card bus system comprising: a plurality of cards coupled to a card bus;

a host device coupled to the card bus, controlling the card bus system;

(LaBerge teaches of host device north bridge 34 of figure 2 coupled to a plurality of cards, such as modem 46, display controller 43, and I/O controller 54)

a device storing bus occupancy rates for the cards and a variable bus occupancy rate for increasing or decreasing the bus occupancy rates;

(LaBerge teaches in figure 5 of configuration register 63 that comprise bus occupancy rates, COL. 4, lines 40 – 59).

and a bus arbiter controlling a priority for use of the card bus in accordance with the bus occupancy rates for the cards in response to interrupt signals generated by the cards.

(LaBerge teaches of bus arbiter 42 of figure 2 that comprises the elements illustrated in figure 5 that would respond to the interrupts from processor 32, COL. 2, lines 32 – 45).

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher A. Daley whose telephone number is 571 272 3625. The examiner can normally be reached on 9 am. - 4p m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571 272 3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul R. Myers

PAUL R. MYERS
PRIMARY EXAMINER

CAD
10/14/2005